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06EC74

Seventh Semester B.E. Degree Examination, June/July 2011
DSP Algorithms & Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions selecting at least TWO questions from each part.***

PART – A

1 a. Explain a digital signal processing system with the help of a block diagram. **(08 Marks)**

b. The signal shown in the following figure is to be sampled. Determine the minimum sampling rate without any aliasing effect. If the signal is sampled at a rate 8 kHz, determine the cut off frequency of the anti-aliasing filter. **(06 Marks)**

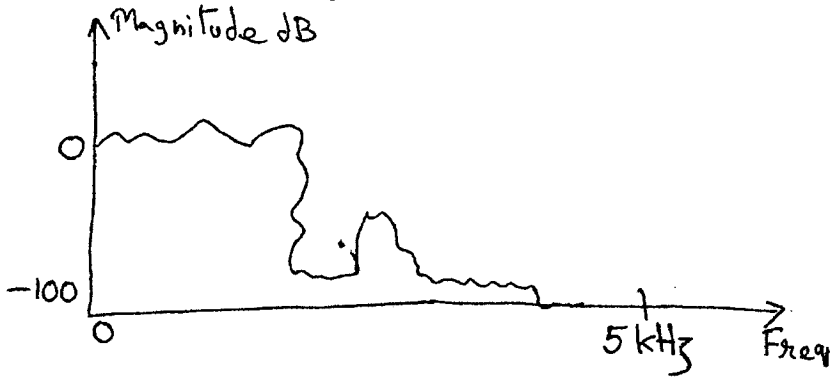

Fig. Q1 (b)

c. Explain with the help of mathematical equations, how signed numbers can be multiplied. **(06 Marks)**

2 a. Implement a 3-bit shift right, barrel shifter. Tabulate the outputs for different bit shifts. **(10 Marks)**

b. 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow? **(03 Marks)**

c. Discuss the role of saturation logic. Explain its function with the help of a block diagram. **(07 Marks)**

3 a. Implement an 8 tap or 8 co-efficients FIR filter using a single MAC unit and other standard blocks. **(04 Marks)**

b. Discuss any three data addressing modes of a TMS320C54XX processor. Give one example for each mode. **(09 Marks)**

c. Explain sequential and other types of program control. **(07 Marks)**

4 a. Find out the contents of accumulators A, B and T register after execution of each of the following instructions:

i) MAC *AR5+,#0123h, A

ii) MPY #0123, A

Initial contents in both the cases are as follows:

A 010h,	AR5	0410h
0410h 10h	T	020h
0411h 11h	B	030h

(10 Marks)

b. Show the pipeline operation with the help of a table, for the following sequence of instructions if the initial value of AR3 is 81 and the values stored in memory location 81, 82, 83 are 1, 2 and 3 respectively. Also tabulate the contents of AR3 and A at the end of each cycle.
Instructions:
LD*AR3+,A
ADD #1000h, A
STL A, *AR3+ **(10 Marks)**

PART – B

5 a. What values are represented by the 16 bit fixed point number N = 2000 h in the Q0, Q7 and Q15 notations? **(09 Marks)**

b. Explain with the help of a block diagram and mathematical equations, the implementation of a second order IIR filter. No program code is expected. **(11 Marks)**

6 a. Sketch a signal flow graph for a general butterfly computation. **(04 Marks)**

b. Derive the expressions for computation of outputs of the butterfly sketched in Q6 (a). **(06 Marks)**

c. Determine the optimum scaling factor to prevent overflow. **(10 Marks)**

7 a. Sketch the I/O interface signals at the pins $R/\overline{W}$, $\overline{IS}$ and $\overline{IOSTRB}$ for a read-write-read sequence of operations. **(08 Marks)**

b. What is the range of addresses that can be decoded if A19 is pulled low in a processor with 20 address lines? **(06 Marks)**

c. What is interrupt? **(02 Marks)**

d. What are the various classes of interrupts available in the TMS320C5416 processor? **(04 Marks)**

8 a. Explain with the help of a block diagram, how DMA operation is configured. **(05 Marks)**

b. Explain each instruction in the following code:
DMSA, set 55h
DMSDN, set 57h
DMSRC2, set 0Ah

```
STM DMSRC2, DMSA
STM #1110h, DMSDN
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What will be the content of DMSRC2 after execution of this instruction? **(05 Marks)**

c. Explain JPEG encoding and decoding with the help of a block diagram. **(10 Marks)**

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